

XA-9472

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.:

Filed: Herewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT

* * *

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified
application as indicated below.

IN THE CLAIMS:

8. (Amended) A semiconductor integrated circuit
according to claim 6, wherein said first logic gate includes
an MIS transistor to which a substrate bias is applied in a
reverse direction by a potential in said well region, and said
second logic gate includes an MIS transistor to which a
substrate bias is applied in a forward direction by a
potential in said well region.

9. (Amended) A semiconductor integrated circuit
according to claim 6, wherein said first logic gate includes a

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D. Bell
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